

---

## Design of a Recording System for a Muon Telescope Using FPGA and VHDL

---

S. Yasue,<sup>1</sup> K. Munakata,<sup>1</sup> C. Kato,<sup>1</sup> T. Kuwabara,<sup>1</sup> S. Akahane,<sup>1</sup> M. Koyama,<sup>1</sup>  
Z. Fujii,<sup>2</sup> P. Evenson,<sup>3</sup> and J. W. Bieber,<sup>3</sup>

(1) *Department of Physics, Shinshu University, Matsumoto 390-8621, Japan*

(2) *Solar-Terr. Env. Laboratory, Nagoya University, Nagoya 464-8601, Japan*

(3) *Bartol Research Institute, University of Delaware, Newark, DE 19716, USA*

---

### 1. Abstract

A prototype multi-directional muon detector has been in operation at São Martinho in Brazil, since March, 2001. We now plan to extend the detector in size to a full scale detector comparable to the Nagoya muon telescope. We have started to design a new recording system using the FPGA and VHDL. By using the FPGA and VHDL, it becomes possible to design a more complicated and advanced logical circuit at a reduced cost. As the result, we can determine the incident direction of every single muon and record the count rates in the total 121 incident directions. It is also noted that the power consumption can be decreased drastically.

### 2. Introduction

We have installed the prototype multi-directional muon telescope at the INPE's Southern Space Observatory (Geographic Lat: 29.44°S, Long: 53.81°W, Alt: 500 m) at São Martinho in Brazil, on March, 2001 [1]. It is confirmed that the pitch angle coverage of the network is greatly improved by this new detector in Brazil [1,2], because the former network consisting of Nagoya, Hobart and Mawson had a big gap in directional coverage over the Atlantic and European region, and this gap was filled by the new detector in Brazil [3]. It is concluded, however, that the extension of the Brazilian detector in size is required for more precise and reliable observations [1].

We are now planning to extend the detector size to a full scale size comparable to the Nagoya muon telescope (6×6 array of 1 m<sup>2</sup> detectors). We have started to design a new recording system using the devices of Field Programmable Gate Array (FPGA) and VHSIS Hardware Description Language (VHDL) for the full-scale muon telescope. By using the FPGA and VHDL, it becomes possible to design a more complicated and advanced logical circuit at a reduced cost, which could not be accomplished by the conventional system using the logic gate ICs.

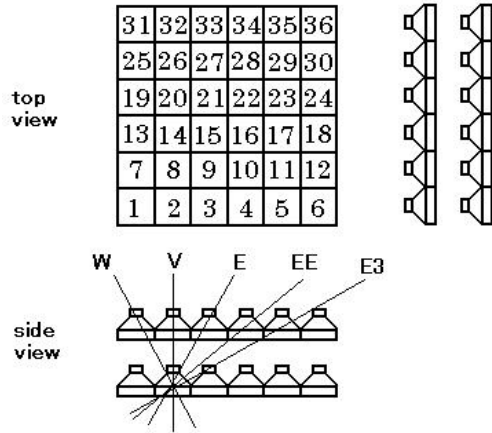


Fig. 1. Arrangement of the new detector.

### 3. The New Muon Telescope

Arrangement of the new muon detector (top view and side views) is shown in Fig. 1. The total seventy-two (36×2) detectors will be placed in two layers (upper and lower) separated vertically by 1.73 m. Each detector consists of a 1m<sup>2</sup> plastic scintillator with 10 cm thickness, and a 5-inch photo-multiplier tube. Numbering of each detector is also shown in this figure. The incident direction of W-, V-, E-, EE-, and E3-directional channels are also illustrated. The incident direction will be determined in two different ways in the new recording system using the FPGA and VHDL. One is based on the conventional and traditional logic, and the other is based on a new logic. The new logic becomes possible only by using the FPGA and VHDL. These two logics are explained below.

### 4. The Conventional Logic

The conventional logic for determining the incident direction is based on the two-fold coincidence between the pulses coming from the upper and lower detectors. For example, North (N) telescope is composed of 30 two-fold coincidences, as

$$\begin{aligned}
 N = & (U7 \times L1) + (U8 \times L2) + \dots + (U12 \times L6) \\
 & \dots \dots \dots \dots \dots \dots \dots \dots \dots \\
 & + (U31 \times L25) + (U32 \times L26) + \dots + (U36 \times L30).
 \end{aligned}$$

Where ‘×’ and ‘+’ denote ‘AND’ and ‘OR’, and U and L represent upper and lower layer, respectively. Numbering of detectors is shown in Fig. 1. The coincidence system produces 29 directional components in total, including V, N, E, S, W, NE, ES, SW, WN, NN, EE, SS, WW, N3, E3, S3 and W3. Fig. 2 shows one segment of logical circuit used in the two-fold coincidence system. The VHDL description

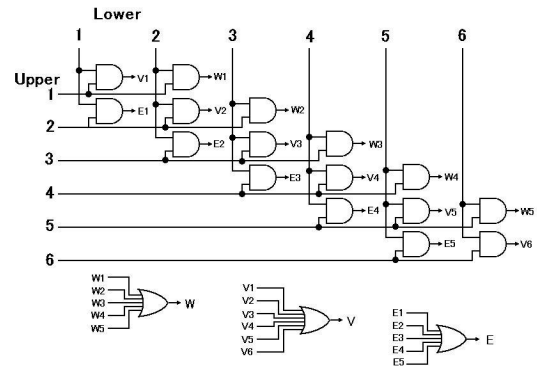
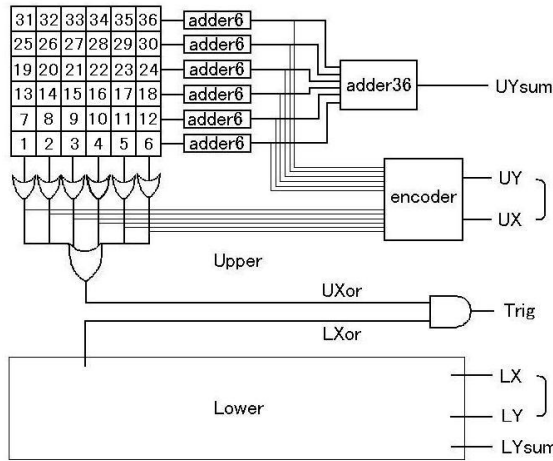
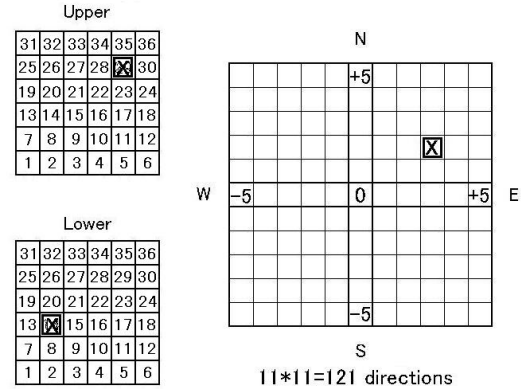


Fig. 2. One segment of the coincidence circuit.



**Fig. 3.** The block diagram of the new logic.



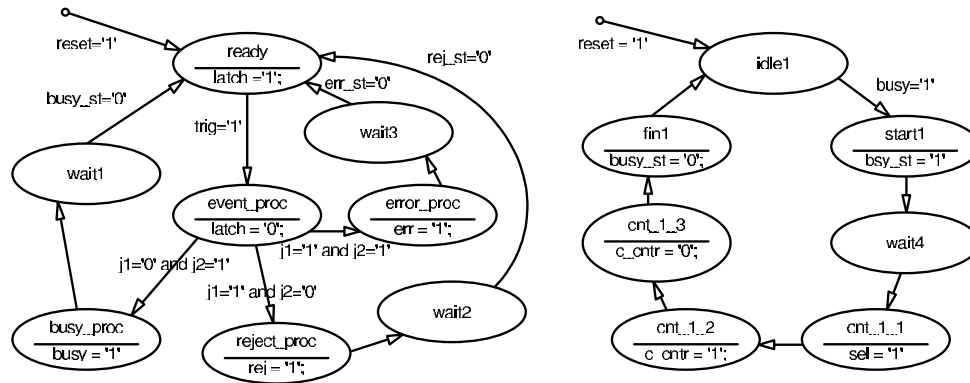
**Fig. 4.** Position of detected muon (left) and corresponding incident direction (right).

of this circuit is easily made based on this logical circuits. It is noted that all these circuits plus counters can be configured in only one device of the FPGA.

### 5. The New Logic

Fig. 3 shows the new logic for the determination of the incident direction. When a particle arrives and passes through the upper and lower layers, output signals from the detectors produce the signals, UXor and LXor shown in the figure. The coincidence between UXor and LXor produces an event trigger signal. The following successive operations are triggered by this event trigger signal.

1. All input signals (72 in total) from all detectors are latched and retained until the analysis of the event is finished.
2. Total number of the output signals from the upper layer is calculated in adder circuits consisting of “adder6” and “adder36”, and appears at UYsum in the diagram. At LYsum in the figure, appears the total number of signals from the lower layer. UYsum and LYsum are 6-bit vectors.
3. Values of UYsum and LYsum are examined in the comparator. In order to get a unique incident direction, the operation determining the incident direction is started only in the case of UYsum=1 and LYsum=1.
4. We can obtain the position of the detected muon (UX, UY) of the upper detector. Similarly, the position (LX, LY) of the lower detector are also obtained. Making the differences, UX-LX and UY-LY, we can determine one incident direction, as shown in Fig. 4.
5. When the operation determining the incident direction is started, a single incident direction is determined out of 11×11=121 possible directions, and a count pulse is fed to the corresponding counter (see Fig. 4).



**Fig. 5.** State diagrams producing control signals. (Left) On detecting a trigger signal, busy-process is started. (Right) Every step of busy-process proceed in 100 nS.

Fig. 5 shows the state diagram producing control signals. The process of event analysis is started by the detection of the event trigger signal, and is finished by the count pulse produced from the above operation 5. As shown in the figure, the time required for analyzing one event is about one micro second, which is short enough for the ground-based muon detector and the dead time is negligibly small. Each counter circuit consists of a 4-digits BCD counter, a latch circuit, and a tri-state buffer. One device of FPGA, for example XC2S200 from Xilinx, can store as many as 32 channel counters. Thus, by using only four devices, we can record the count rate of 121 directions necessary for the new method.

It is emphasized that another advantage in using FPGA is the low electricity consumption. Our tentative use of FPGA revealed that the consumption of electricity for one device is small enough comparing to the conventional circuits. As a large amount of logical circuits are configured in one device of FPGA, the total consumption of electric power is expected to be decreased drastically.

## 6. Acknowledgements

This work is supported by the joint research program of the Solar-Terrestrial Environmental Laboratory, Nagoya University.

## 7. References

1. Munakata K. et al. 2001, Proc. 27th ICRC 9, 3494.
2. Munakata K. et al. 2003, Proc. 28th ICRC (in this issue).
3. Munakata K. et al. 2000, J. Geophys. Res. 105, 27,457.